

Discrete Maths - Digital Logic

Laboratory 2: Karnaugh Maps

2007 September 14 edition

Assessment Criteria

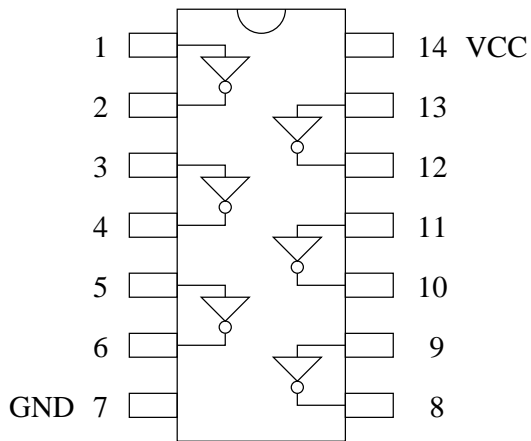
Assessment in this lab is based on these performance measures:

1. Mastery of Boolean Logic;
2. Adherence to Design Principles;
3. Circuit construction;
4. Record of results;
5. Tidying up after yourself.

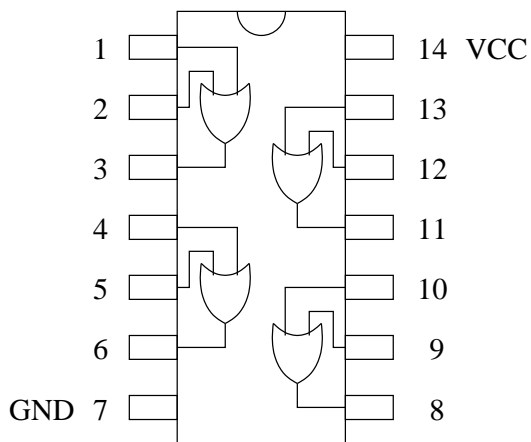
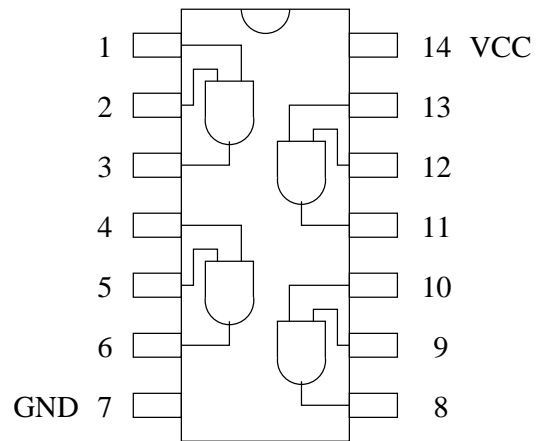
1 Equipment List

1. 5V power supply
2. Protoboard
3. I/O board
4. Cutters
5. Pliers
6. Single strand hook-up wire
7. 74LS04 (Inverter) integrated circuit
8. 74LS08 (AND)
9. 74LS32 (OR)
10. 74LS86 (XOR)

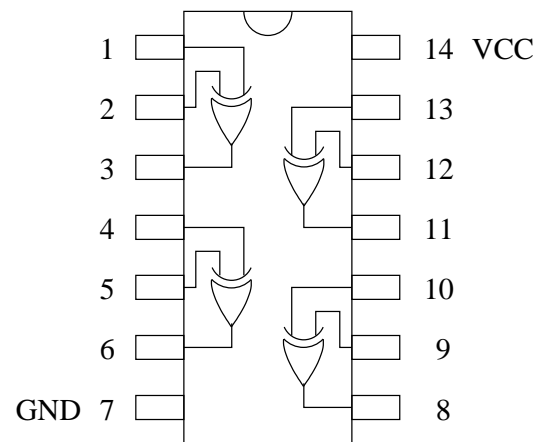
74LS04 HEX NOT



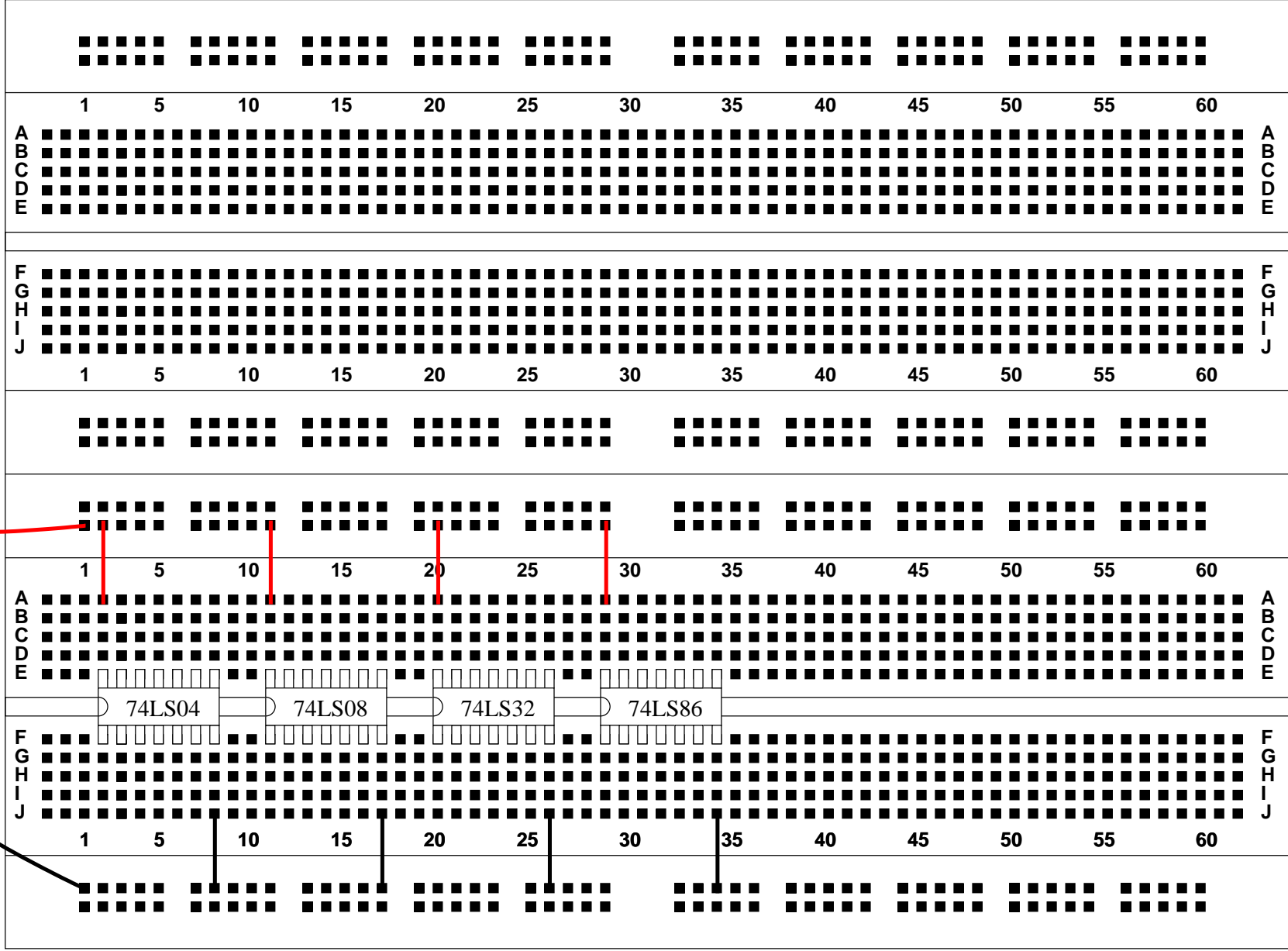
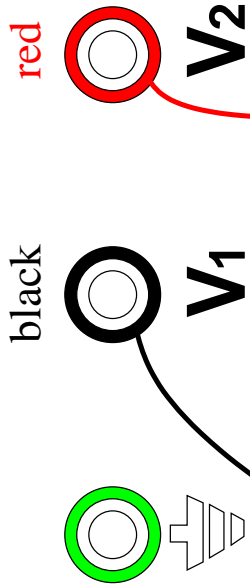
74LS08 QUAD AND



74LS32 QUAD OR



74LS86 QUAD XOR



2 Simplifying Boolean Logic using Karnaugh Maps

A **sum of products** (OR of AND terms), also known as **disjunctive normal form (DNF)**, Boolean expression $Z = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C} + ABC$ has this **Karnaugh map**:

Z	AB	$\bar{A}B$	$\bar{A}\bar{B}$	$A\bar{B}$
\bar{C}	1	0	1	1
C	0	0	1	0

- On the map above, form **groups** by using a **pencil** to draw **rectangles** containing **1s** to **minimise** the logic.

Hint 1: You only need two (yes, 2) groups.

(Sure, you can see 3 groups, but one of them is redundant because all its 1s are covered by the other two groups.)

*Hint 2: A good heuristic method for minimisation of small cases such as this involves trying to **cover all the 1s** with as **few** groups as possible, and with each group as **large** as possible.*

*Explanation: Because of the **binary** nature of Boolean logic, each group **must** be a **rectangle** containing a **power of two** number of 1s (but **no** 0s).*

- Then, in the space below, write the minimal expression.

Z =

That expression is called a **simplified sum of products (SSOP)**, also known as a **minimal disjunctive normal form (minimal DNF)**.

- Draw the **logic gate diagram** of this expression in the following space.
- Write **pin numbers on all inputs and outputs of every gate.**

- **Identify** the two intermediate signals that I've named X and Y: what **combination of A, B and C** are they?
- Choose a **color** for each signal, thus completing this color table:

Signal	A	B	C	\bar{A}	\bar{B}	\bar{C}	X =	Y =	Z
Color									

- Write its **color** next to each **signal line** in the above **circuit diagram**.
- **HAVE YOU completed all the work above?**
- **NO? Then GO BACK and FINISH IT!**
- **HAVE YOU COMPLETED THE DIAGRAM YET?**
- **YES? IF so,** you may **NOW construct** the circuit.
- **Test** the circuit, recording each **OBSERVED** output in this truth table:

A	B	C	Z
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

KEEP this circuit! You NEED it for the next section!

Has a demonstrator marked you yet?

You do want the marks, don't you?

3 Don't Care States (compare Tocci, chapter 4)

A digital circuit is often part of a larger system, in the normal operation of which *some* Boolean input combinations do *not occur*. These "don't care" conditions are indicated by an "X" in the output column of the truth table. Here's an example:

A	B	C	Z
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	X
1	0	0	X
1	0	1	1
1	1	0	0
1	1	1	0

- Fill in the Karnaugh map for that logic:

Z	\bar{C}	C
$\bar{A}\bar{B}$		
$\bar{A}B$		
AB		
$A\bar{B}$		

- Now replace each X by a 0 or 1 value (possibly different for each X) to simplify the Karnaugh map:

Z	\bar{C}	C
$\bar{A}\bar{B}$		
$\bar{A}B$		
AB		
$A\bar{B}$		

- **Group 1s** to minimise the logic.
- What is the corresponding SSOP expression?

Z =

- **ASK a demonstrator for the SIMPLEST way to use the PREVIOUS circuit to implement this expression!** (Hint: all you need do is SWAP two (2) wires at the switch sockets.)
- After swapping the two wires, test the circuit, recording your **OBSERVED results** in this truth table:

A	B	C	Z
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Have you been marked for this circuit?

4 Half Adder

4.1 Using Karnaugh maps

When we add two single-bit inputs, A and B, we obtain a two-bit answer, CS. The carry bit is the more significant (bit 1), and the sum S is the less significant (bit 0).

- Complete the following combined truth table.

A	B	C	S
0	0		
0	1		
1	0		
1	1		

- Fill in the Karnaugh maps for C and S:

C	\bar{B}	B
\bar{A}		
A		

S	\bar{B}	B
\bar{A}		
A		

- Group the 1s in each Karnaugh map to minimise the logic.

Hint: When simplifying NOT, AND and OR logic, remember that grouping of 1s can occur horizontally and vertically (unless a 0 blocks the way), but *not* diagonally.

- How many groups are there in C? *Answer:*
- How many groups in S? *Answer:*
- How many 1s in each group? *Answer:*
- Can you *simplify* the logic? *Answer:*
- Write the minimal disjunctive normal form expressions for C and S:

C =

S =

- Draw the (2-input, 2-output) **logic circuit** that implements this **half adder** (in the next outlined space).
- Label both its **inputs, A and B**, as well as its *two* **outputs, C and S**.
- Label A and B with their **switch numbers**.
- Label C and S with their **LED numbers**.
- Write the **pin numbers** on every gate's input(s) and output in your **circuit diagram**.

- Now **identify** the circuit's four *intermediate* signals (which I've labelled **V, W, X** and **Y** below) and **label them** on the **circuit diagram** above.
- Choose a **color** for *every* signal, completing the table below:

Signal	A	B	V =	W =	X =	Y =	C	S
Color								

- **WRITE** the name of its **COLOR** next to **each SIGNAL LINE** in your **circuit DIAGRAM**.
- **Have you drawn and labelled EVERYTHING, as instructed? If not, do it NOW!**
- **ONLY THEN** may you **construct** the circuit, using the **eight colors** you have **chosen**.
- Test the circuit, and record the observed values of **C** and **S** in this truth table:

A	B	C	S
0	0		
0	1		
1	0		
1	1		

Has a demonstrator marked you for this yet?

4.2 Another implementation

- Express **S** using a **single logic gate**. (*Hint: It's an **XOR**, or Exclusive OR gate. If you're not familiar with the XOR operation in Boolean logic, or don't know its **mathematical symbol**, then ask a demonstrator.*)

S =

- C** already only uses a single gate (**which gate?**), so the expression for **C** remains as:

C =

- Draw the new **logic diagram** for the **half adder**, including **both** outputs **S** and **C** (in the next outlined space).
- If you don't know the **electronic logic symbol** for an **XOR** gate, then **ask a demonstrator**.
- Include **pin numbers** on all inputs and outputs of each gate.
- Include **switch numbers** at the circuit inputs **A** and **B**, and **LED numbers** at the outputs **C** and **S**.

- Choose a **color** for each signal:

Signal	A	B	C	S
Color				

- Write the name of its **color** next to each **signal line** in your **circuit diagram**.
- IF** you've done ALL that, THEN you may **construct** the circuit, test it, and record the observed values of C and S:

A	B	C	S
0	0		
0	1		
1	0		
1	1		

5 Cleaning Up

- All ICs must stay on the board.
- Both protoboard and I/O board and all borrowed tools (pliers and/or cutters and/or meters) must **remain** on your bench for a demonstrator to collect.
- Please ensure that every **cord**, **wire**, is returned to its proper place, that all instruments are switched off, that your **bench** and its environs, including the **carpet**, are **clean**, and that your **seat** is placed under the bench.

Edition: 2007 Sep 14 Fri 12:24 Geoffrey Tobin