

2 Electronic Logic Symbols

In digital electronics there is a wide range of building blocks called logic elements. These are predefined circuits which perform specified logic functions. When drawing an element, its symbol denotes its function. (It does *not* describe the internal structure of an electronic circuit that may be used to implement each element.)

Standardisation is important for a quick and clear understanding of the function of the circuits. Once the underlying rules are understood, symbols for complex digital integrated circuits can be constructed.

The international standard for electronic logic symbols is documented in the International Electrotechnical Commission's IEC 617 series, *Graphical Symbols for Diagrams*. (See <http://www.iec.ch> which is the IEC's website.)

The conformant Australian standards are detailed in the document series:

- AS1102-1989, *Graphical symbols for electrotechnical documentation*;
- AS3702-1989, *Item designation in electrotechnology*.

These are produced by Standards Australia Limited (<http://www.standards.org.au>) and are obtainable through the SAI Global WebShop at <http://saiglobal.com> which provides both PDF and hard copies (at a price of around \$50 per document).

All symbols for logic blocks are based on a rectangular 'box' representation. Symbols for basic logic elements such as AND gates, OR gates and inverters are also drawn in this form. This is often foreign to the shaped symbols commonly used to represent these basic elements.

2.1 Terminology

It is useful to define some basic terms:

Internal logic state

A logic state which exists inside the symbol outline at an input or output.

External logic state

A logic state which exists outside the symbol outline at an input or output. Note that if external qualifying symbols exist, then this logic state is before the qualifying symbol for an input and after the qualifying symbol for an output.

Positive logic convention

H (high) level represents the logic 1-state and L (low) level represents the 0-state. This is the usual convention.

Logic element

An element whose outputs are defined digital functions of the inputs.

General qualifying symbol

Symbol placed within the element outline to define the function of that element.

Qualifying symbol

A symbol which operates on the inputs or outputs as they enter or leave the element outline. (An example of a use of a qualifying symbol is to indicate the inversion of a signal).

2.2 Purpose of Logic Symbols

Logic symbols often appear unduly complex. However they should contain sufficient information to avoid the need to refer to the manufacturer's data when attempting to understand the circuit concept. Another reason for complexity is the need to specify manufacturing/testing information such as pin numbers.

Information regarding the internal operation of a logic element can often be omitted if it has no direct relevance to the overall circuit function. The objective is to use concise representation of the function without any irrelevant information.

2.3 Conventions

General Qualifying Symbols

Table 1 gives a list of general qualifying symbols used to label logic elements. The symbols should be placed inside the rectangular logic symbol as shown in figure 1. The item designation, the device type and the location are also shown however these are outside the symbol.

Qualifying Symbols

Table 2 gives a list of qualifying symbols which operate on inputs or outputs, or define the way in which an input or output functions. Figure 1 shows inversion of the output of a three input AND gate forming a NAND gate. Symbols other than inversion are placed inside the rectangular logic symbol adjacent to the input or output to which they refer.

Signal Flow

Where possible, signal flow should be from left to right and from top to bottom.

Symbol Spacing

To assist in clarifying the function of a logic element, the element can be segmented into the basic functional blocks which are adjacent to one another each with a general qualifying symbol as shown in figure 2.

Note that where there are identical symbols it is permissible to only label the first (top) symbol as shown in figure 2.

Where there is insufficient room the draw interconnections between separate elements, symbols can be cascaded as seen in figure 2.

Common Control Blocks

Where inputs are common to all elements in a device a common block is placed at one end of the array of elements as shown in figure 3.

Detached Elements

For circuit clarity it is often useful to detach elements of a device to different sections of the circuit diagram. This is accomplished in a semi-detached manner as shown in figure 4. Fully detached representation is shown in figure 5 where each detached set of elements is labelled with the item designator.

Common Output Elements

These are drawn as a sub-element of the common control block as shown in figure 6.

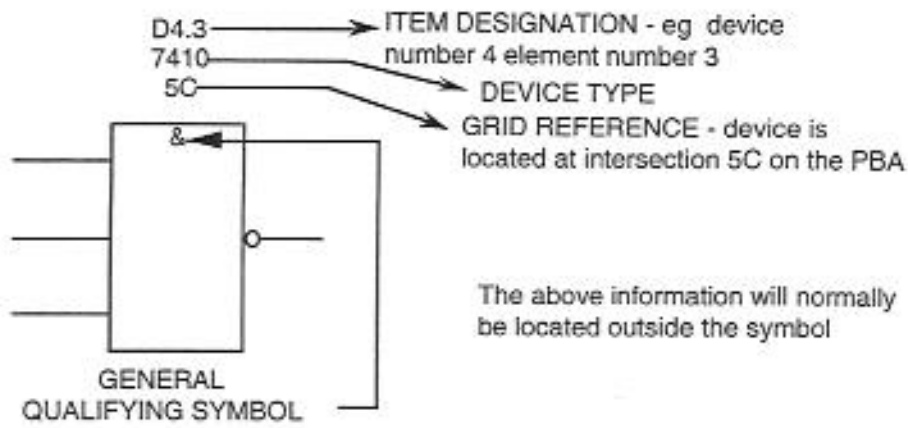


Figure 1: Example of 3 input NAND Gate

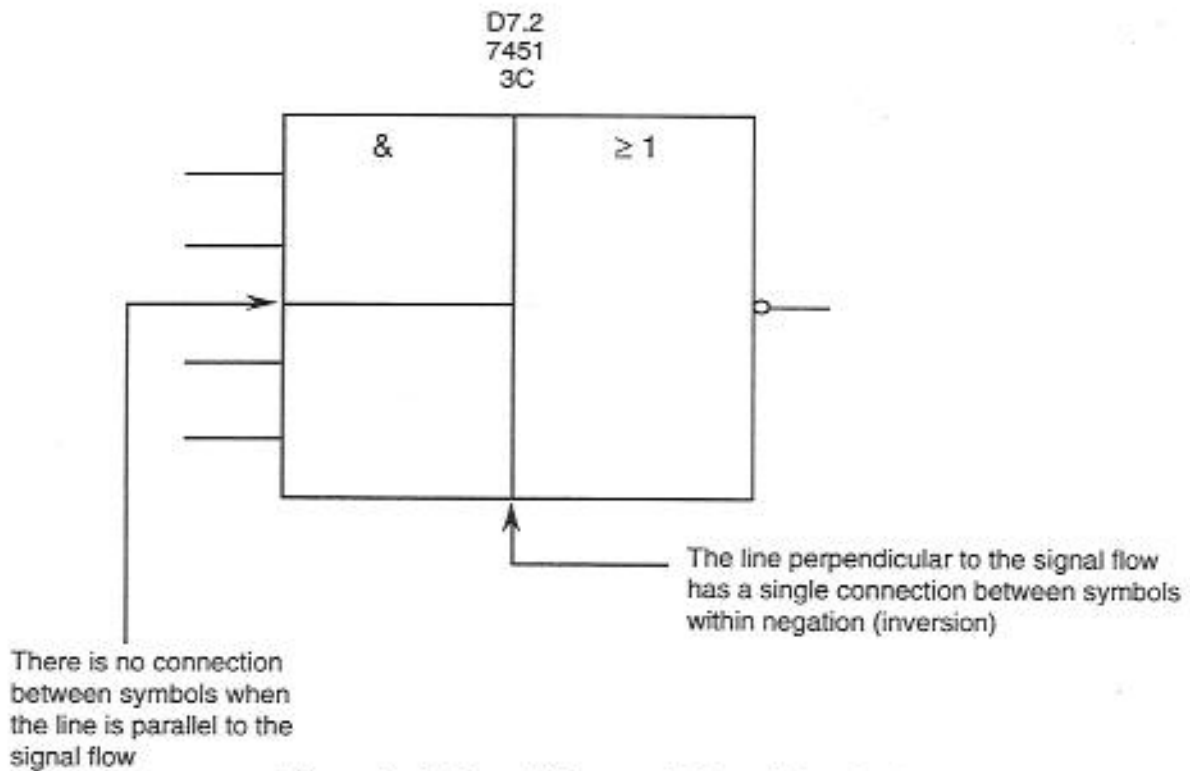


Figure 2: Internal Segmentation of Symbols

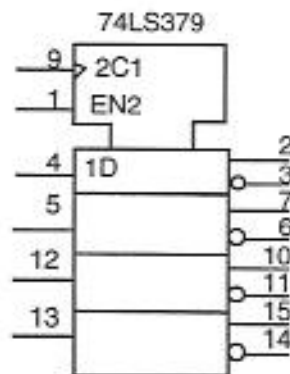


Figure 3: Common Control Block

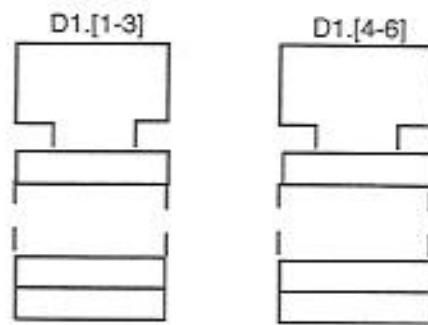


Figure 4: Semi-detached Elements

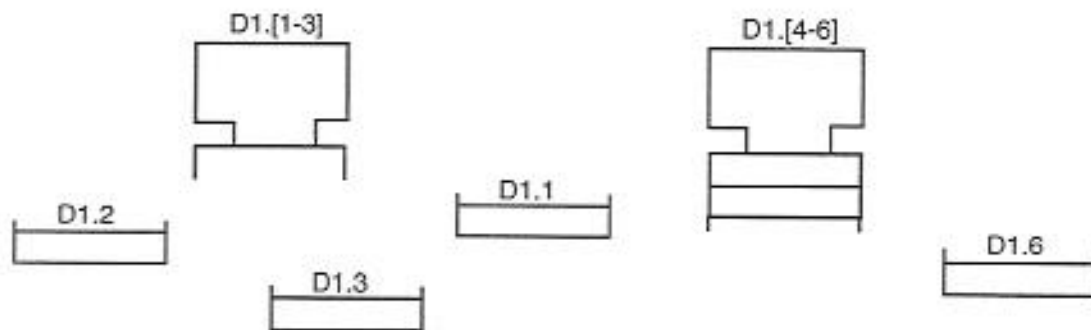


Figure 5: Fully-detached elements

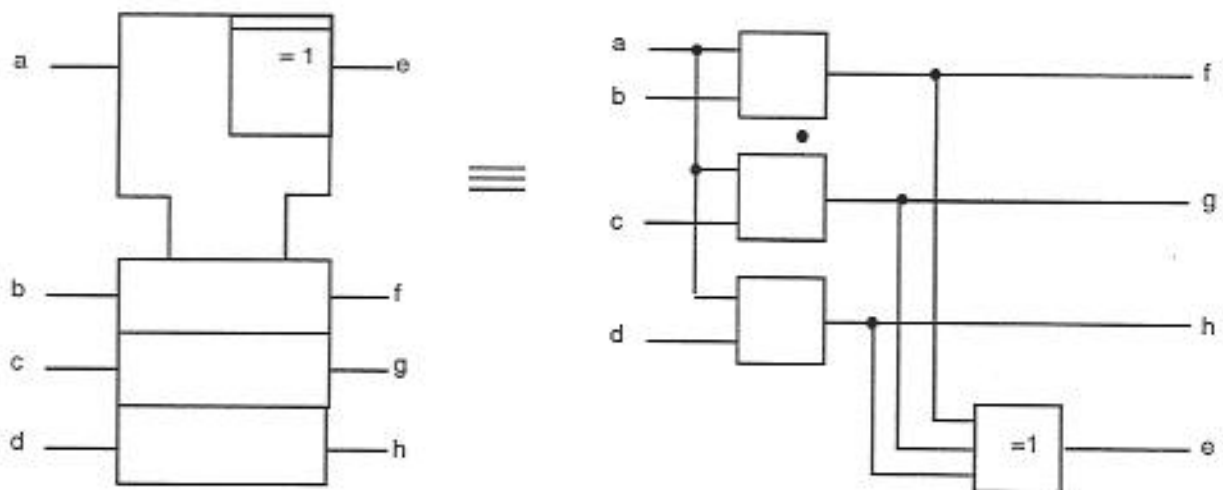


Figure 6: Common output block

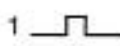




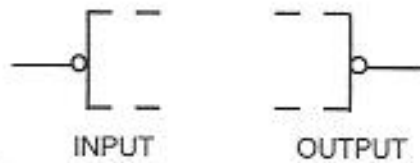
1	&	AND gate	15	CPG	Look-ahead carry generator (Carry Propagate & Generate)
2	≥ 1	OR gate	16	Σ	Adder
3	1	Buffer (inverting or non-inverting)	17	Π	Multiplier
4	= 1	Exclusive OR gate	18	COMP	Comparator
5	1 	Monostable retriggerable) (non-	19	ALU	Arithmetic Logic Unit
6		Monostable (retriggerable)	20	XX	Cross-connected switch
7		Amplifier (buffer)	21	BCD/DEC	Coder (BCD to decimal)
8		Delay element	22	BIN/7.SEG	Coder (Binary to 7-segment)
9	ROM	Read Only Memory	23	HPR/BIN	Coder (Highest Priority to Binary)
10	EPROM	Erasable Programmable Read Only Memory	24	EX 3 GRAY/DEC	Coder (Excess-3-Gray to Decimal)
11	RAM	Random Access Memory (Read/Write Memory)	25	RTX	Transceiver
12	MUX	Multiplexer	27	CTR	Counter
13	DMUX	Demultiplexer	28	DIV	Divider
14	P-Q	Subtractor	29		Astable

Table 1: General qualifying Symbols for Identifying Logic Symbols

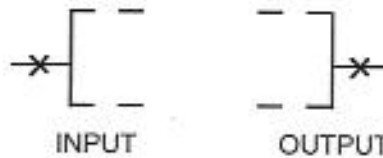
Function

Qualifying Symbol

Inversion

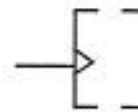


NON-LOGIC INPUT/OUTPUT

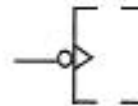


Dynamic input
(edge sensitive)

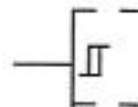
Positive edge active



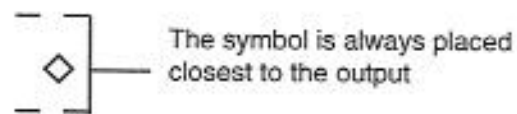
Negative edge active



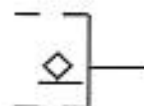
Schmitt trigger input



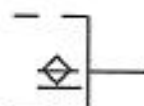
Open-circuit symbol



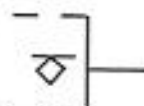
Open-collector/drain
(pull-down)



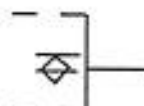
with internal pull-up



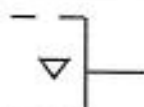
Open-emitter/source
(pull-up)



with internal pull-down



3-state output
(0,1 or high impedance)




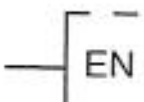
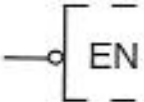

D Input (data input)	
EN input (enable outputs)	
active low	
Postponed output (flip-flop outputs)	

Table 2: Symbols used for qualifying inputs or outputs