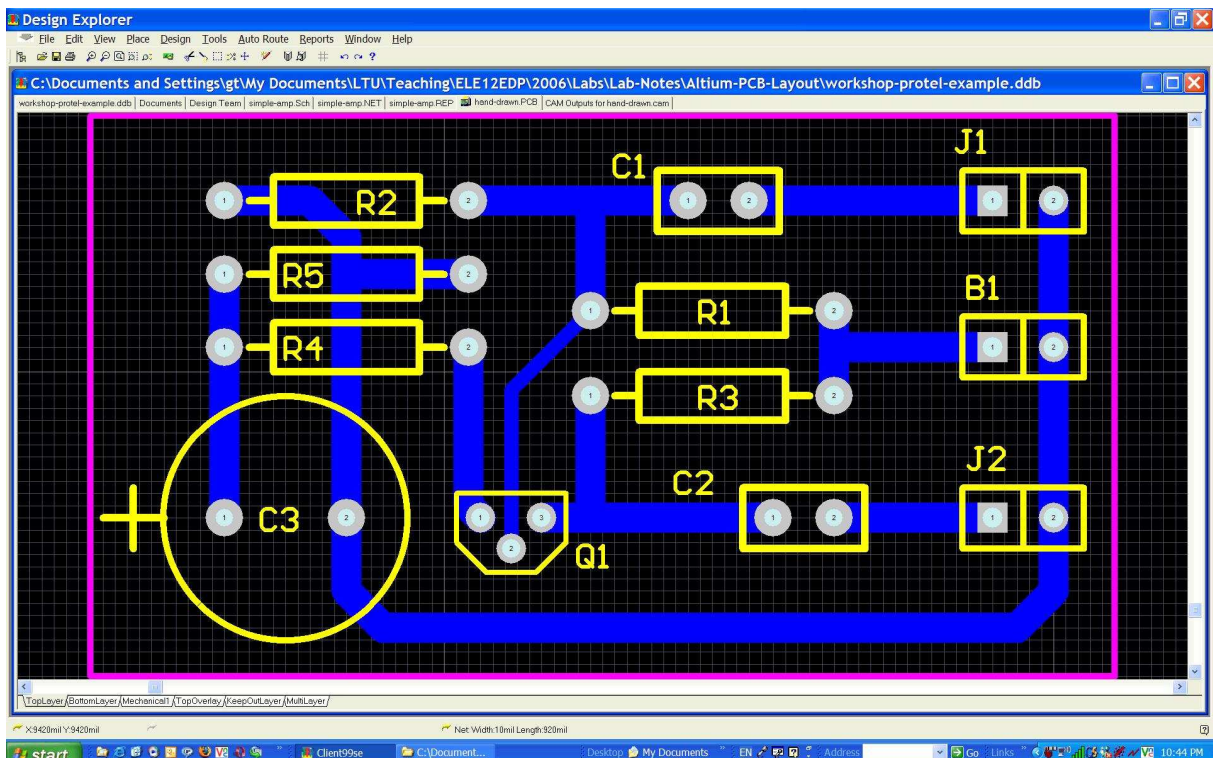


ELE1EDP: Electronic Design Project

2007 Laboratory:

Altium PCB Layout

- Login to a computer.
- Create the folder **H:\ELE1EDP\PCB**
- Start up Altium 6.7.
- **File -> New -> PCB.**
- **Save As ... Hand-Drawn** in the **H:\ELE1EDP\PCB** folder.
- Remember to **Save** every five (5) minutes.
- Study this screen capture of a PCB layout which used an older version of this software.



- This particular PCB design uses three layers:
 1. **Keep Out Layer** for drawing the **Keep Out Boundary Line** (magenta).
 2. **Top Layer** for placing **components** (yellow).
 3. **Bottom Layer** for drawing the **tracks** (blue).
- Right click on the PCB and change the **Snap Grid** to **20 mil**.

- Select the **Keep Out** Layer. Using **PL** (for **Place Line**), carefully draw a boundary rectangle that is **1680 mil** wide by **920 mil** high.
- Select **Edit -> Set Origin**. Place the new origin at the bottom left corner of the Keep Out boundary.
- Note that, by default, all component and track measurements are reckoned in **mils** (milli-inches!) as the electronic industry's IC and PCB standards originate from the USA.
- Change the **Snap Grid** to **50 mil**.
- Select the **Top** Layer. Place the components, using **PC** (short for **Place Component**). Choose the **footprints** given in the following table. For example, the five resistors have AXIAL-0.4 as their footprint, so place one AXIAL-0.4 with the name R1, then place four more. Altium will name these R2 to R5 in order. Similarly for the other components. Note: in this design, we leave the comment field blank.

Footprint	Designators
AXIAL-0.4	R1 to R5
RAD-0.1	C1, C2
RB-5/10.5	C3
HDR-1X2	B1, J1, J2
TO-92A	Q1

- Components can be **moved** by **clicking** and **dragging**.
- Change the **size** of all **designators** using **Edit -> Change**. Set the **height** to **35 mil** and the **width** to **6 mil**. Click **Global**, then **OK**. Move all the designators to match the picture above.
- Change the **Snap Grid** to **5 mil**.
- Select the **Bottom** Layer.
- Most of the tracks are have **Width 50 mil**, but the thin one connecting the base of Q1 to the left pad of R1 has **Width 24 mil**.
- Change the permitted track widths for the bottom layer to a **minimum** of **24 mil**, a **typical** value of **50 mil**, and a **maximum** of **50 mil**.
- Draw the tracks, using **PT** (short for Place Track).
- When you have finished drawing, turn **off** the design rule for Electrical Shorts.
- Run a Design Rule Check: **Tools -> Design Rule Check -> Run DRC**. If there are any errors, you must correct them.
- **Save** your file.
- When your PCB layout is complete, show it to a demonstrator for marking.
- **Logout**, then **shut down** the computer, then **switch off the monitor**, before leaving.

Geoffrey Tobin

Version **8**

Tuesday **14 August 2007**

END.