

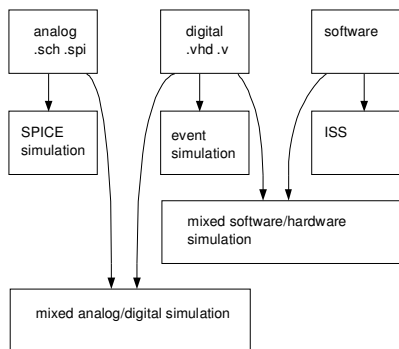
INTEGRATED CIRCUIT DESIGN

Dragan Stancic

Outline

- Overview of IC Design
 - Review tools environment
 - IC Design Flow
 - System Level Design
 - Architectural Exploration
 - Design Partitioning
 - RTL Level Design
 - High Level Languages
 - Hardware Description Languages
 - Tools Integration

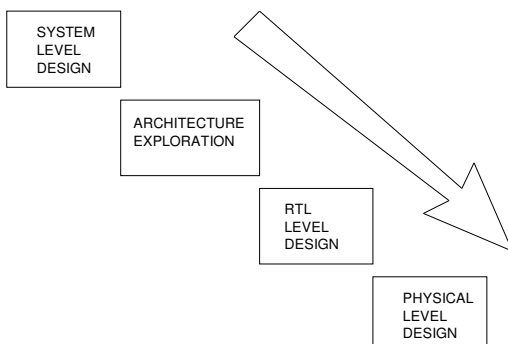
IC Design Flow



IC Design Flow

- System Level Design
- Architecture Exploration and Partitioning
- RTL Design and Implementation (digital)
- Analog Design
- Physical Implementation

IC Design Flow



System Level Design

- High level languages
 - C/C++
 - Matlab
 - Behavioural VHDL/Verilog
 - System Verilog
 - SystemC
 - other
- Graphical Entry
 - FSM, Flow chart, Structural and Data diagram, ..
 - Tool specific

Architectural Exploration

- Manual process
- Few tools available
- Tools not mature

Design Partitioning

- Manual Process
- Moving functionality into entities
- Splitting analog/digital
- Splitting software/hardware

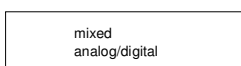
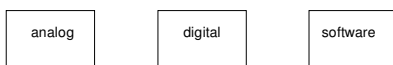
RTL Level Design

- Commonly used
- HDL Languages
 - VHDL, Verilog
 - SystemC
 - other
- Graphical entry
 - FSM, Flow chart, Block diagrams, ..
 - Tool specific

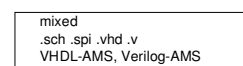
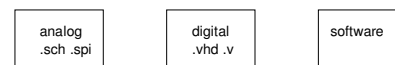
Physical Level Design

- Manual Analog Design
- Manual floor planning and partitioning
- Automated Place & Route

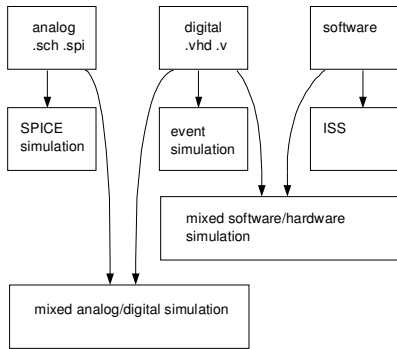
IC Design Flow



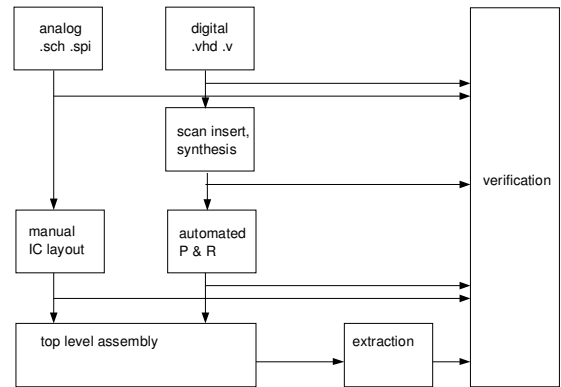
IC Design Flow



IC Design Flow



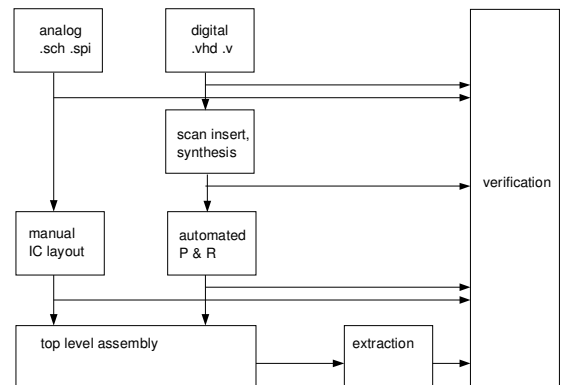
IC Design Flow



Modeling

- Primitives models
- Macro models
- VC models

EDA Tools



Analog Design

- Schematic entry
- SPICE models
- SPICE simulation

HDL Design

- Textual
 - VHDL, Verilog, ..
- Graphical
 - FSM, Flow Chart, Structural Diagram, ..
- Rule checker

HDL Simulation

- Event driven
- HDL Language support
- Mixed HLL and HDL support
- Code debugging
- Regression testing
- Code Coverage

Mixed Analog/Digital Simulation

- Synchronisation of event between simulators
- Language support
- Mixed language support

Software/Hardware Co-Simulation

- Simulation acceleration
- Emulation
- Language support
- Processor support

Behavioural Synthesis

- Architecture exploration
- Resource allocation
- Scheduling
- Language support

RTL Synthesis

- Technology support
- Language support
- Hierarchy manipulation

Scan Insertion

- DFT rule checker
- Manufacturability
- Yield

Static Timing Analyzer

- Timing violations
- Technology support

Logic Equivalence Checker

- Accelerated verification
- Verification coverage

Analog Place & Route

- Device generators
- Technology support

Floorplan

- Top level assembly

Digital Place & Route

- Technology support
- Density

Design Rule Checker

- Design rules violations
- Functional errors
- Shorts

Logic Versus Schematic

- Extract cells
- Correlate with design intent

Tools Integration

- Time to Market
- Simulation accuracy
 - Support for mixed simulations

Tools Integration

- Compatibility:
 - with standards
 - with other tools
 - with tools from other EDA vendors

Tools Integration

- Abstraction levels
 - Translation accuracy
 - Manual translation across abstraction levels

Tools Integration

- Language support
 - HLL and HDL support
 - Analog, digital and mixed support
 - Software and hardware support